AMENDMENTS TO THE DRAWINGS

Please replace the earlier submitted Replacement Drawing Sheet 9/13 relating to Fig. 12 of the drawings, which was submitted in the Amendment of March 27, 2006, with the current Replacement Drawing Sheet 9/13, and, also, please replace the original Drawing Sheet 10/13 related to Fig. 14 of the Drawings, which are enclosed herewith in Appendix G. Regarding the further Replacement Sheet for Drawing Sheet 9/13, the current revision thereto is in supplement to the earlier revision made with regard to the Amendment filed on March 27, 2006. Acceptance of the currently submitted Replacement Sheets directed to Figs. 12 and 14 is respectfully requested. The current revisions being made in Figs. 12 and 14 concern the removal of inadvertently made [nodal] connection indicators in those drawings as can be seen in the Annotated Drawing Sheets directed to Sheets 9/13 and 10/13, covering Figs. 12 and 14. Regarding Fig. 14 of the drawings, the inadvertent electrical connection points between the upper row read-out line and each of the common drain lines 76 were appropriately removed, consistent with the showings in the lower row of memory cells of the frame memory. Likewise, similar such connection points between the vertical drain lines (which are grounded by the common drain line 66) and the respective read-out lines of both of the shown rows of memory cells of the frame memory in Fig. 12 were appropriately deleted. These revisions, it is submitted, remove obvious minor informalities.

Attachments:

Appendix G: Further replacement sheet for Drawing sheet 9/13 and a replacement sheet for original Drawing sheet 10/13; and

Appendix H: Annotated Drawing sheets directed to Sheets 9/13 (Fig. 12) and 10/13 (Fig. 14).

REMARKS

Reconsideration and allowance of the above-identified application, as currently amended, is respectfully requested.

Acceptance/formal entry of the accompanying further replacement sheet for prior Drawing replacement sheet 9/13 as well as acceptance of replacement sheet for original Drawing sheet 10/13 is respectfully requested. As indicated under the heading Amendment to the Drawings, these replacement sheets correct minor informalities in connection with the originally presented Drawing sheets. The corrections made involve the removal of inadvertently drawn electrical connection points, as shown in the annotated sheets. The removal of these connection points removes the inadvertent shorting of the read-out line and the common drain line, consistent with that shown elsewhere in Fig. 12 as well as in other ones of the illustrated example embodiments. It is submitted, the current revisions being made to the Drawings are also strictly of a minor formal matter and, therefore, acceptance and formal entry of the current replacement sheets for Drawing sheets 9/13 and 10/13 is respectfully requested.

The earlier submitted Second Substitute Specification (submitted as an Attachment to the Amendment filed on April 10, 2006) is being further amended to correct discovered informalities therein. It appears that these informalities resulted in connection with the preparation of the originally submitted Substitute Specification which also involved a change in font type. Additionally, a revision of a clarifying nature, involving a minor interlineation, is also included with the current revisions being implemented. Regarding the latter, a parenthetical expression is being added in paragraph [0046] to highlight the fact that a refresh operation to a memory cell of a frame memory according to the

invention is actually a re-write operation performed to refresh the stored data. Although this should be clearly understood from the detailed description of the Specification such as with regard in paragraphs [0045]-[0049], regarding the example embodiment shown in Fig. 1+ of the Drawings, although not limited thereto, the parenthetical insertion was effected, nonetheless, for purposes of such emphasis. It is submitted, this change is strictly of a minor editorial nature, not altering the original scope or intent of the Specification, and, therefore, acceptance of the same is respectfully requested. It is submitted, also, the changes being effected with the filing of the Third Substitute Specification do not include new matter, either by addition/or deletion. Therefore, entry of the Third Substitute Specification (Appendix I) is respectfully requested. A marked-up version thereof (which includes revisions to the earlier submitted Second Substitute Specification) is also enclosed herewith (see Appendix J).

By the above-made amendments, also, claims 1-39 remain pending, of which claims 28 and 29 were further amended. The amendments effected therein, however, are strictly of a minor editorial nature. Specifically, in independent claim 28, the expression "each display pixel comprises ..." now reads as "each display pixel comprising ...". With regard to independent claim 29, also, the expression "each display pixel a pixel electrode ..." now contains the missing term comprising so that it appropriately reads as "each display pixel comprising a pixel electrode ...", consistent with similar such recited expressions contained in the other independent claims. As is clearly apparent, these revisions are strictly of an editorial formatting/correcting nature. Discussion will now turn to the rejections.

All of the currently pending claims were rejected over the same combination of references as that earlier applied. Namely, claims 1, 9, 11, 14-17, 21-23, 25, and 29-39 were rejected under 35 USC § 103(a), allegedly, as being unpatentable over the combination of Yamaguchi, et al. (U.S. Patent 5,627,557) in view of Booth, Jr., et al., hereinafter Booth, et al. (U.S. Patent 6,642,945); claims 2-8, 10, 18-20, 24, and 27 were rejected under 35 USC § 103(a), allegedly, as being unpatentable over the combination of Yamaguchi, et al. in view of Booth, et al., as applied to claims 1, 9, 11, 14-17, 21-23, 25, and 29-39, and further in view of Parks (U.S. Patent 5,471,225); and claim 28 was rejected under 35 USC § 103(a), allegedly, as being unpatentable over the combination of Yamaguchi, et al., supra, in view of Zhang, et al. (U.S. Patent 6,611,261). As will be shown below, the invention set forth in claims 1-39 was not taught nor could have been realizable even in view of the combined teachings of the art documents, as applied in these rejections. Therefore, these rejections are traversed and withdrawal of the same is respectfully requested.

A key aspect according to each of independent claims 1, 29, 31, 32, 33, 35, 36, 37, and 39 and, correspondingly, of the dependent claims thereof concerns the refreshing operation of the memory cells of the image display apparatus according to the present invention. The refreshing operation is actually a re-write operation to effect a refreshing of the written data on a memory cell such as with regard to the memory cells 11 of the frame memory shown in the example Fig. 1+ embodiment of the present application, although not limited thereto.

According to independent claim 1, for example, the invention is an image display apparatus, an example of which is shown in Fig. 1+, although not limited thereto, which calls for, among the featured aspects thereof:

> wherein each basic unit of a memory element comprises a memory switch; a memory capacitor connected to said memory switch; an amplifier field-effect transistor (FET) of which a gate is connected to said memory capacitor; and refreshing operation means for performing a preset refreshing operation to rewrite a signal charge stored in said memory capacitor using said amplifier FET.

An example operation of the embodiment according to Figs. 1-8 is given in paragraphs [0045]-[0047], et seq. of the present Specification. In accordance with this example embodiment and, also, with regard to other ones of the disclosed example embodiments, the image data representing the stored data in the memory capacitor of the memory cell of the framed memory that is outputted to the corresponding data line 22, in response to the read-out line 13 signal, is re-written in the same memory capacitor 31 when the buffer selection switch 16 activates the corresponding word line 12. For example, when the buffer selection switch 16 is switched to the word line buffer 14 to set the word line 12 in that row to the high voltage level, the read image data which is written in the data line 22 is re-written in the same memory capacitor 31. such represents the refresh operation performed to the memory cell, namely, a read-write operation of the stored data of the memory cell is performed to effect a refreshing of that stored data (see in paragraph [0046], lines 10-13 thereof). It is submitted, a scheme is that called for in independent claim 1 and, likewise, with regard to all other ones of the independent claims (which set forth such a schemed refreshing operation means , although presented somewhat differently in different claims) was not taught even in view of the combined teachings of Yamaguchi, et al. and Booth, et al.

It is admitted in the rejection based on the combination of Yamaguch, et al. and Booth, et al. that Yamaguchi, et al. at least does not disclose "a refreshing operation means for performing a preset operation to signal charge stored in the memory capacitor." (Page 3, lines 14-18, of the Substitute Office Action.) In this rejection, however, it is alleged, also, that Booth, et al. discloses such a concept in the details of the respective display elements 120 which include a pixel cell 125 and a storage unit 124, the latter containing a much larger capacitor (e.g., 142) than the capacitor of the Pixel cell. Regarding the "refresh", Yamaguchi, et al. discloses a concept in which new data is written in the picture element (the Pixel). Yamaguchi, et al.'s scheme, it is observed, is intended for "an analog" memory and that written-in data is data written newly. Storage levels associated with such an analog memory, as that typified in Yamaguchi, et al.'s schemed construction, leads to loss of data resulting from leakage current over time. In accordance with the present invention, however, each basic unit of a memory cell such as of a frame memory in an image display apparatus comprises a memory switch, a memory capacitor connected to the memory switch, an amplifier FET, and refreshing operation memory means for performing a preset refreshing operation to re-write a signal charge stored in the memory capacitor using the amplifier FET, the signal charge stored being in the form of digital display data. An example of this is briefly discussed above regarding the performing of a preset refreshing operation to re-write stored digital data such as in a multi-bit memory element as that shown in Figs. 1 and 2 of the Drawings in conjunction with the timing chart illustrated in Fig. 8. According to the present invention, by effecting a re-writing (re-write) operation of the data stored in the memory cell, many times, it therefore becomes possible to preserve or maintain semi-

permanently, the written data. Such concept was neither disclosed by Booth, et al. nor could have been suggested in view of the combined teachings of Yamaguchi, et al. and Booth, et al.

In accordance with the discussion in column 5, lines 6-42, in Booth, et al., it is alleged in the rejection that "it would have been obvious ... to allow the usage of the update circuit including the capacitor for refreshing the voltages in the pixel cell arrangement which is taught by Booth, in a device ... taught by Yamaguchi, et al. ..." to realize the invention according to base claim 1 and, likewise, according to each of the other independent claims and, therefore, also according to the corresponding dependent claims thereof. A careful study of Booth, et al.'s disclosure shows that Booth, et al. teaches a scheme in which a loss of analog data, caused by leakage current over time, is mitigated. Booth, et al.'s scheme does not involve in a refresh operation to recover data or reliably re-write data such as presently set forth and as explained with regard to the various example embodiments of the present application. According to Booth, et al, the display panel (see Figs. 5 and 6) is such that a terminal voltage of the pixel uses analog memory and that written-in data is strictly data that is newly written. In other words, Booth, et al., applicants submit, does not teach a refreshing operation scheme for performing a preset refreshing operation to re-write stored digital display data in the manner as that set forth in base claim 1 and, likewise, with regard to other ones of the independent claims and further according to the corresponding dependent claims thereof.

In accordance with the present invention, the concept of a preset refreshing operation in a digital memory resides in the recovery by re-writing, in the data, which is done repeatedly until newly inputted data is written in the memory, in which case the newly written data is now maintained through

employing the preset refreshing operation according to the present invention. As emphasized above, since Booth, et al.'s scheme does not employ the function for re-writing (to re-write data in the manner defined in independent claims 1,29.31-33,35-37 and 39), the data according to Booth, et al.'s scheme would clearly become lost over time. On the other hand, the stored data according to the present invention, it is submitted, would be maintained as a result of repeated re-writing operations effected by the "refreshing operation means".

The invention according to dependent claims 2-8, 10, 18-20, 24, and 27 is also considered patentable even when Yamaguchi, et al. and Booth, et al. are combined with Parks, et al., for the same and similar reasons as that argued above. In this regard, it is noted that Parks was cited concerning the Pixel construction and other structural particulars of a liquid crystal display. That is, the above deficiencies regarding the combined teachings of Yamaguchi, et al. and Booth, et al. are not overcome even in view of the further teachings of Parks.

Regarding the image display apparatus according to independent claim 28, a featured aspect thereof calls for the set forth "reference voltage generating circuit" of the "image signal generating means" to employ a boron-doped poly-Si thin film resistor. Such, it is submitted, is not taught even in view of the combined teachings of Yamaguchi, et al. and Zhang, et al. As correctly noted in the rejection, Yamaguchi, et al. fails to teach a display apparatus in which the image signal generating means has a reference voltage generating circuit using a poly-Si thin film resistor to achieve a gray scale voltage generating resistor. Zhang, et al, also, does not disclose or suggest a specific doping characteristic regarding the poly-Si thin film used therein. It is

submitted, when applying the combined teachings of Yamaguchi, et al. and Zhang, et al., it is apparent that the resistance used in attaining an analog standard voltage may be prepared using a poly-Si thin film in which phosphorous and arsenic and the like are doped. On the other hand, in accordance with the present invention, the poly-Si thin film resistor of the present invention is a boron-doped poly-Si thin film resistor [having low-dispersion sheet resistance] which leads to unexpected favorable results as that compared with, for example, phosphorous doped poly-Si material (with regard to the formation of the thin film resistor). Such favorable attributes directed to a boron-doped poly-Si thin film resistor according to the invention set forth in independent claim 28 are discussed in paragraph [0040] in conjunction with Table 2, beginning on page 11 of the Specification. Such a schemed construction, it is submitted, is not taught from the combined teachings of Yamaguchi, et al. and Zhang, et al.

For purposes of this response, relevant supportive discussion/rebuttal arguments presented in previously submitted responses are also incorporated herein for purposes of the present response.

Therefore, acceptance of the above-made amendments as well as reconsideration and withdrawal of the outstanding rejections and favorable action on the currently pending claims and an early formal Notification of Allowance of the above-identified application is respectfully requested.

Statement of Substance of Interview

The Examiner's summation in the interview summary form (PTOL-413) received as an attachment to the outstanding Substitute Office Action is correct and, therefore, additional comments directed thereto are unnecessary. The

Examiner is thanked for her courteousness during the held telephone interview on July 7, 2006.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned representative at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including Extension of Time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (503.40029X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

Larry N. Anagnos
Reg. No. 32,392

LNA/mlh
Telephone: (703) 312-6600
Facsimile: (703) 312-6666

FIG. 12

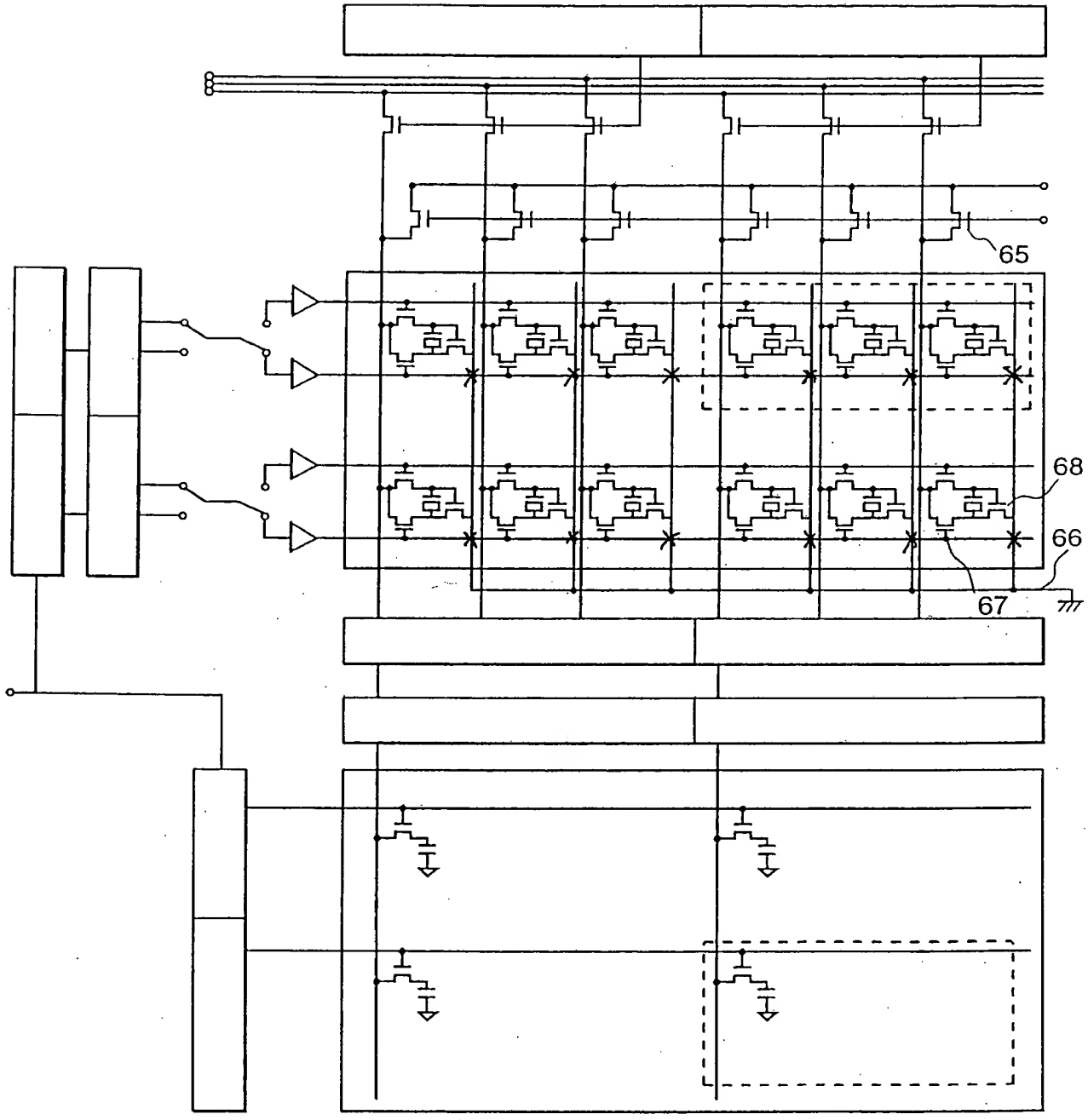

FIG. 14